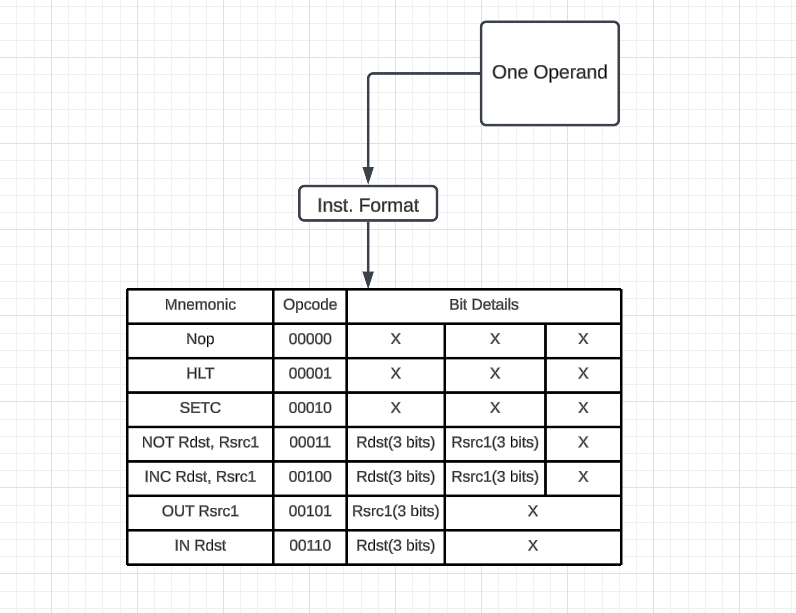
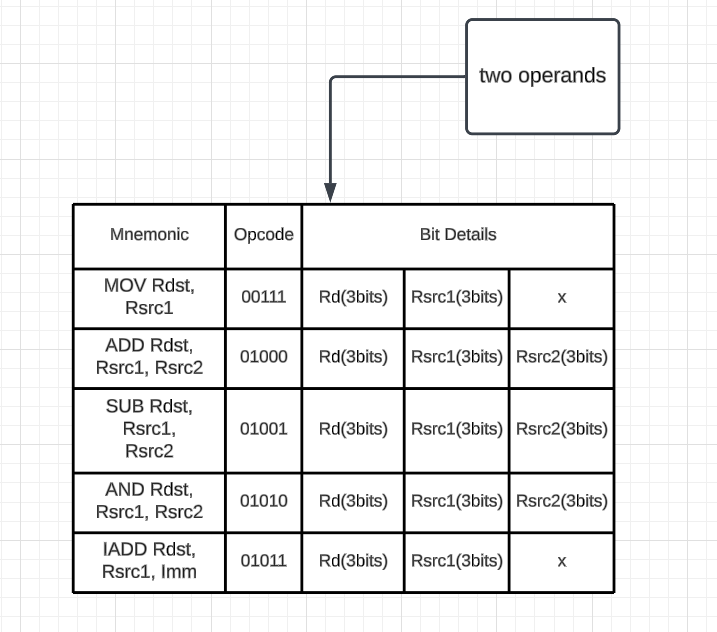
**Computer Arch. Project  
Phase 1**

**Team Members:**

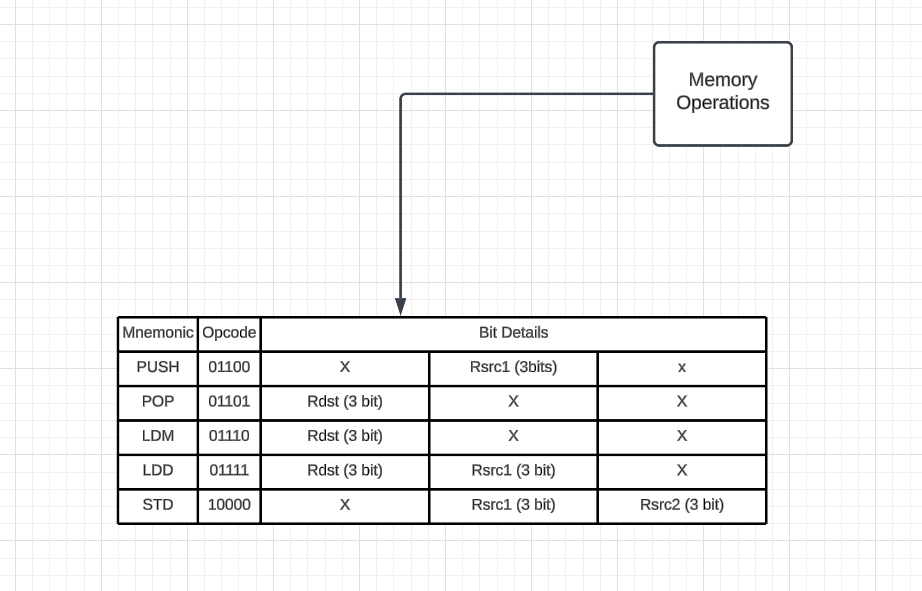
* Kirollos Baghdad (9210859)
* Mohammed Abd Elaziz Abdo Khater (9220713)
* Ahmed Kamal (9220075)
* Ahmed Mostafa Ali Bakr (9220111)

**Instruction Format**

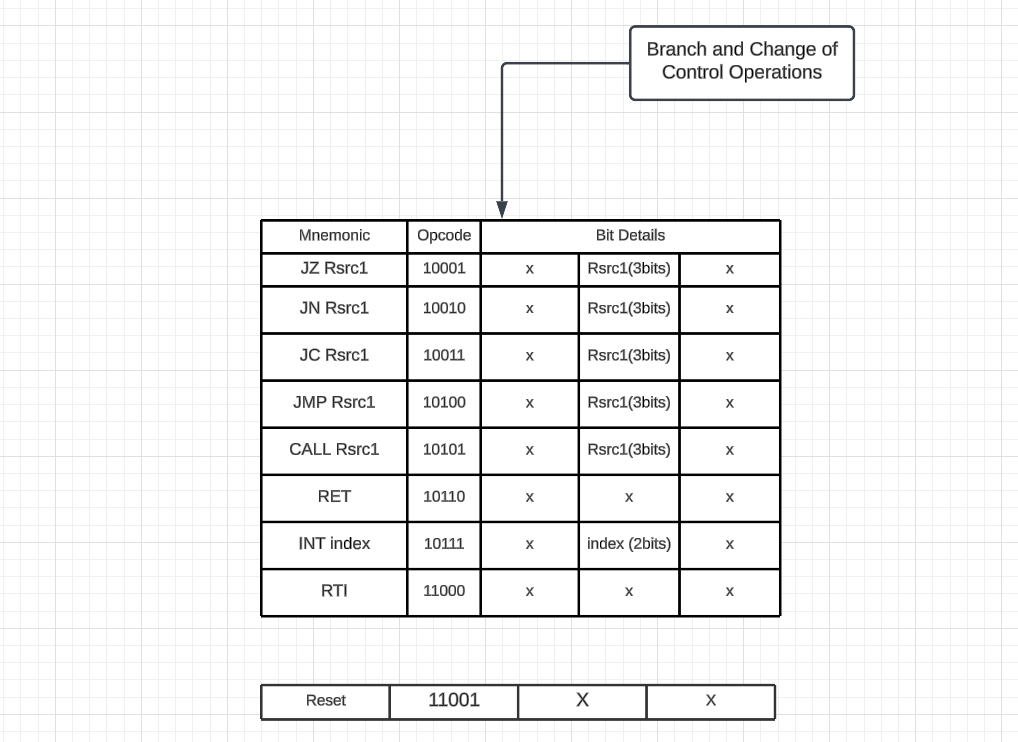
1 ) One Operand



2) Two Operand

3) Memory Operations

4) Branch & Change of Control Signals

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**Schematic diagram of the processor**Link for LucidChart Schematic:

[Arch Project: Lucidchart](https://lucid.app/lucidchart/053da06d-fdec-4601-980f-ece1d0313f1a/edit?invitationId=inv_e930c4f7-df32-464c-adbd-8af895294b1c&page=0_0)

**Pipeline stages design**

Pipeline registers details

1. F/D Register
   * Inputs & Outputs: Instruction [15:0], Updated PC [15:0], User Input [15:0], Reset, Flush
   * Size: (16 + 16 + 16 + 1 + 1) = 50 Bits
2. D/E Register
   * Inputs & Outputs: R1 [15:0], R2 [15:0], User Input [15:0], Flush, Updated PC [15:0],  
     Control Signals (Mread, Mwrite, WB, Alu [2:0], branch, MemtoReg, Instr/Immd, Stack, Call, Pop, LDM, RET, RTI, Store, LDD, Zero, IN, enable), Rdst [2:0]
   * Size: (16 + 16 + 16 + 1 + 16 + 22 + 3) = 90 Bits
3. E/M Register
   * Inputs & Outputs: AluResult [15:0], br\_taken, Updated PC [15:0], Rsrc1 [15:0], Flush, Rdst [2:0], Control Signals(Mread, Mwrite, WB, MemtoReg, Stack, Call, Pop, LDM, RET, RTI, Store, LDD, enable)
   * Size: (16 + 1 + 16 + 16 + 3 + 14) = 66 Bits
4. E/WB Register
   * Inputs & Outputs: Updated PC [15:0], ReadData [15:0], Updated SP [15:0], Rdst [2:0], AluResult [15:0], Rsrc1 [15:0],  
     Control Signals(WB, MemToReg, Stack, enable)
   * Size: (16 + 16 + 16 + 3 + 16 + 16 + 4) = 87 Bits

**Pipeline Hazards**

* **Data Forwarding**
  + Full Forwarding
* **Static Branch Prediction**
  + Branch is predicted as NOT-TAKEN
  + Branch is checked in the ALU Stage
  + In case of branch Taken, the (F/D, D/E, E/M) registers are flushed

**DONE**